REMARKS

Claims 1, 2, 3, 8, 9, and 10 are pending and under consideration. Claim 4 is canceled herein without prejudice or disclaimer. This amendment is believed to place the application in condition for allowance, and entry thereof is respectfully requested. In the alternative, entry of this amendment is requested as placing the application in better condition for appeal by, at least, reducing the number of issues outstanding. Further reconsideration is requested based on the foregoing amendment and the following remarks.

Response to Arguments:

The Applicants appreciate the consideration given to their arguments, and the new grounds of rejection. Further favorable consideration is requested.

Claim Rejections - 35 U.S.C. § 112:

Claims 1, 2, and 3 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The final Office Action, in particular, asserts that the recitation "by using phase information on a data signal which is not used by said phase comparator circuit before detecting said absence," is not described in the specification. The rejection is traversed.

According to one method of performing a phase comparison by using a clock having a frequency which is half of the data rate, all of the phase information is not utilized. Rather, only half the phase information is utilized, as described at page 8, lines 17-20 of the specification as filed originally, with reference to Figs. 6 and 7. The method is described in further detail at page 7, lines 20-37, continuing at page 8, lines 1-14.

In Fig. 7 is shown a case in which a phase comparison cannot be achieved, even though the signal (1) has phase information. The reason for this is that only a part of the phase information of the data signal is used, i.e. the whole of the phase information of the data signal is not utilized. Fig. 7, for example, shows a data signal of "11001100...". In this case, the method tries to use the phase information of the data signal defined between "1" and "1" and between "0" and "0" first, without using the phase information of the data signal defined between "1" and "0" and between "0" and "1." However, since there is no transition of data in the former case, and therefore there is no phase information, the phase comparison cannot be achieved.

Fig. 6, in contrast, shows a case in which phase information of the data signal defined between "1" and "0" and between "0" and "1" is utilized. The phase information of the data signal defined between "1" and "1" and between "0" and "0," however, are not utilized.

A transition from a first state to a second state, finally, is shown in Fig. 11 and described at page 14, lines 9-34 of the specification. The first state is a state in which "a phase comparison cannot be achieved, although the signal (1) has phase information." The second state, on the other hand, is a state in which a phase comparison can be achieved, as in Fig. 6, with the use of phase information which was not utilized previously, i.e. "by using phase information on a data signal which is not used by said phase comparator circuit before detecting said absence," as recited in claim 1.

Claims 1, 2, and 3 are thus submitted to comply with the written description requirement within the meaning of 35 U.S.C. § 112, first paragraph. Withdrawal of the rejection of claims 1, 2, and 3 is earnestly solicited.

Claim Rejections - 35 U.S.C. § 103:

Claims 1, 2, and 3 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the section of the subject application entitled Background Art in view of U.S. Patent No. 5,956,370 to Soda (hereinafter "Soda"). The rejection is traversed to the extent it would apply to the claims as amended. Reconsideration is earnestly solicited.

In the claimed invention, synchronization is maintained by using phase information on a data signal. The phase information is inherently not used by a phase comparator circuit. The phase information, however, is used when the phase information is lost for some reason by the phase comparator circuit, which normally operates with the use of a part of the phase information. The preamble of claim 1, in particular, now recites:

> A timing extraction circuit which uses a Phase Locked Loop (PLL) circuit containing a phase comparator circuit performing a phase comparison, by using a part of phase information on a data signal between a data signal of bit rate B (bits/s) and a clock signal of B/2 (Hz) at intervals of 2/B (sec).

Thus, in the claimed invention, all of the phase information is not used. Every other one bit of phase information, rather, is used on the data signal. Neither the section of the subject application entitled "Background Art" nor Soda, on the other hand, teach, disclose, or suggest a "timing extraction circuit which uses a Phase Locked Loop (PLL) circuit containing a phase

comparator circuit performing a phase comparison, by using a part of phase information on a data signal between a data signal of bit rate B (bits/s) and a clock signal of B/2 (Hz) at intervals of 2/B (sec)," as recited in claim 1.

The second clause of claim 1 recites:

> A detection circuit detecting the absence of an output of phase comparison information from said phase comparator circuit by receiving a data signal of a prescribed pattern.

Neither the section of the subject application entitled "Background Art" nor Soda teach, disclose, or suggest "a detection circuit detecting the absence of an output of phase comparison information from said phase comparator circuit by receiving a data signal of a prescribed pattern," as recited in claim 1. The final Office Action seeks to compensate for this deficiency with respect to the Background Art by combining the Background Art with Soda, saying at the bottom of page 4 that:

> In analogous art, Soda teaches a PLL circuit comprising a detection circuit for detecting the absence of an output of phase comparison information from said phase comparator circuit by receiving a data signal of prescribed pattern; and a control circuit for controlling upon detecting said absence, the phase of said clock signal in order to maintain synchronization (see figure 2, component 23 and column 4, line 14 - 33).

Here, the final Office Action analogizes the recited "absence of an output of phase comparison information" to a loss of synchronization. This is submitted to be incorrect. An "absence of an output of phase comparison information," rather, means a *possibility* of the PLL losing synchronization. This means that the loss of synchronization has not yet actually taken place, but will take place if the current state is left as it is without any control.

In Soda, moreover, the synchronism indication signal is continuously *indicative* of collapse of synchronism between the circuit input and output signals, not absent. In particular, as described at column 4, lines 22-29:

> When the synchronism indication signal is continuously indicative of collapse of synchronism between the circuit input and output signals longer than a predetermined time interval which is not shorter than the pull-in time, the oscillation control signal adjusts the oscillation frequency range in accordance with a state of the synchronism indication signal in the manner which will later be described in greater detail.

Since, in Soda, the synchronism indication signal is continuously indicative of collapse of synchronism between the circuit input and output signals, Soda is not "detecting the absence of an output of phase comparison information from said phase comparator circuit by receiving a data signal of a prescribed pattern," as recited in claim 1.

The VCO controller 23 of Soda, in fact, has a timer 51 *responsive* to the synchronism indication signal for timing the predetermined time interval from occurrence of the collapse of synchronism between the circuit input signal and the voltage controlled oscillation signal or the circuit output signal. In particular, as described at column 5, lines 50-56:

> Referring to FIG. 4, an example of the VCO controller 23 comprises a timer 51 responsive to the synchronism indication signal for timing the predetermined time interval from occurrence of the collapse of synchronism between the circuit input signal and the voltage controlled oscillation signal or the circuit output signal to produce a timing signal upon lapse of the predetermined time interval.

Since, in Soda, the timer 51 is responsive to the synchronism indication signal for timing the predetermined time interval from occurrence of the collapse of synchronism between the circuit input signal and the voltage controlled oscillation signal or the circuit output signal, Soda is not "detecting the absence of an output of phase comparison information from said phase comparator circuit by receiving a data signal of a prescribed pattern," as recited in claim 1.

Finally, in Soda, a timing counter 63 begins to count the pulses of the circuit input signal and produces, upon lapse of the predetermined time interval, the timing signal when the synchronism indication signal *indicates* occurrence of collapse of the synchronism between the circuit input signal and the voltage controlled oscillation signal or the circuit output signal, not when it is absent. In particular, as described at column 7, lines 29-37:

> When the synchronism indication signal indicates occurrence of collapse of the synchronism between the circuit input signal and the voltage controlled oscillation signal or the circuit output signal, a timing counter 63 begins to count a count of the pulses of the circuit input signal and produces, upon lapse of the predetermined time interval, the timing signal mentioned in the foregoing.

Since, in Soda, a timing counter 63 begins to count the pulses of the circuit input signal and produces, upon lapse of the predetermined time interval, the timing signal when the synchronism indication signal *indicates* occurrence of collapse of the synchronism between the circuit input signal and the voltage controlled oscillation signal or the circuit output signal, Soda is not "detecting the absence of an output of phase comparison information from said phase

comparator circuit by receiving a data signal of a prescribed pattern," as recited in claim 1. Thus, even if the section of the subject application entitled Background Art were combined with Soda as proposed in the final Office Action, claim 1 would not result.

In the claimed invention, if a data signal of a certain pattern is detected, the current state is moved forcibly to a stable state where a loss of synchronization cannot occur by changing the phase of the clock signal by, for example, π radian. The detected data signal might be, for example, a data signal which is input over a long-term, and has, for example, 1500 bits. Such a data signal may cause a loss of synchronization, even though the loss of synchronization has not yet occurred. The second clause of claim 1, in particular, recites further:

> Before the occurrence of a loss of synchronization at the Phase Locked Loop (PLL) circuit.

Neither of the section of the subject application entitled "Background Art" nor Soda teach, disclose, or suggest "detecting the absence of an output of phase comparison information from said phase comparator circuit. . . before the occurrence of a loss of synchronization at the Phase Locked Loop (PLL) circuit," as recited in claim 1. In Soda, rather, a detecting circuit detects that a loss of synchronization ("collapse of synchronism") has *actually* taken place. In particular, as described at column 9, line 63-67:

> Said synchronism indication signal is continuously indicative of collapse of synchronism between said input and said output signals longer than a predetermined time interval.

Since, in Soda, a detecting circuit detects that a loss of synchronization ("collapse of synchronism") has actually taken place, Soda is not "detecting the absence of an output of phase comparison information from said phase comparator circuit. . . before the occurrence of a loss of synchronization at the Phase Locked Loop (PLL) circuit," as recited in claim 1. Thus, even if the section of the subject application entitled Background Art were combined with Soda as proposed in the final Office Action, claim 1 would not result.

The third clause of claim 1 recites:

> A control circuit controlling, upon detecting said absence, the phase of said clock signal by a change of the phase in order to maintain synchronization, by using phase information on a data signal which is not used by said phase comparator circuit before detecting said absence.

Neither the section of the subject application entitled "Background Art" nor Soda teach, disclose, or suggest "a control circuit controlling, upon detecting said absence, the phase of said clock signal by a change of the phase in order to maintain synchronization, by using phase information on a data signal which is not used by said phase comparator circuit before detecting said absence," as recited in claim 1. Soda, rather, describes a detection circuit for detecting a collapse of synchronization, and a PLL circuit having a control circuit for controlling, in response to the detection of the collapse of synchronization, the oscillation frequency of a VCO, as discussed above. Thus, even if the section of the subject application entitled Background Art were combined with Soda as proposed in the final Office Action, claim 1 would not result. Claim 1 is submitted to be allowable. Withdrawal of the rejection of claim 1 is earnestly solicited.

Claims 2 and 3 depend from claim 1 and add additional distinguishing elements. Claims 2 and 3 are thus also submitted to be allowable. Withdrawal of the rejection of claims 2 and 3 is earnestly solicited.

Allowable Subject Matter:

The Applicants acknowledge with appreciation the allowance of claims 8, 9, and 10.

Conclusion:

Accordingly, in view of the reasons given above, it is submitted that all of claims 1, 2, 3, 8, 9, and 10 are allowable over the cited references. Allowance of all claims 1, 2, 3, 8, 9, and 10 and of this entire application is therefore respectfully requested.

If there are any formal matters remaining after this response, the Examiner is invited to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing this Amendment, please charge them to our Deposit Account No. 19-3935.

Respectfully submitted,

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Date: June 25, 2009

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